Abstract of the Disclosure

A semiconductor memory device including 1T-1C memory cells for increasing an access speed thereto. The semiconductor memory device is composed of a substrate, a MOS (metal oxide semiconductor) transistor formed in a surface portion of the substrate, an inter-level dielectric covering the MOS transistor, a capacitor element, and a contact formed through the inter-level dielectric. The contact electrically connects the capacitor element to the MOS transistor on a source thereof. The contact includes a metal portion formed of metal. The metal portion reduces the resistance of the contact, and thereby increases the access speed of the semiconductor memory device.